

REMARKS

This Amendment is submitted in response to the Office Action dated August 27, 2003, having a shortened statutory period set to expire November 27, 2003.

In paragraph 2 of the present Office Action, the Examiner states that Claims 21-22 have been withdrawn from consideration by constructive election of the originally presented claims. Applicant respectfully traverses the Examiner's restriction because there is no basis for such a restriction in either 37 C.F.R. or the MPEP. In particular, a restriction is only appropriate when "two or more independent and distinct inventions are claimed in a single application." 37 C.F.R. 1.142. In the present case, the claims withdrawn by the Examiner are dependent claims that set forth additional features (i.e., an etch stop layer and conductive via) of the invention recited in the originally presented claims. Accordingly, the inventions recited in Claims 21-22 are not independent of the originally presented invention and are entitled to consideration.

Pursuant to the objections to the specification in paragraph 3 of the present Office Action, Applicant has proposed amendments to the title and abstract. The proposed amendments do not contain any new matter.

Next, in paragraph 7 of the present Office Action, Claims 9 and 14-19 are rejected under 35 U.S.C. § 102(b) as anticipated by U.S. Patent No. 5,742,472 to *Lee et al.* (*Lee*). Next, in paragraph 9 of the present Office Action, Claim 10 is rejected under 35 U.S.C. § 103(a) as unpatentable over *Lee* in view of U.S. Patent No. 4,172,758 to *Bailey et al.* (*Bailey*). Finally, in paragraph 10 of the present Office Action, Claims 11-13 and 20 are rejected under 35 U.S.C. § 103(a) as unpatentable over *Lee* in view of U.S. Patent No. 5,795,819 to *Mostiff et al.* (*Mostiff*). Those rejections are respectfully traversed, and favorable reconsideration of the claims is respectfully requested.

Applicant believes that *Lee*, whether considered alone or in combination with the other prior art references of record, does not render Claim 9 and its dependent claims unpatentable because the cited references do not teach or suggest the combination of features recited in Claim

9. In particular, the cited prior art references do not teach or suggest, “A method of fabricating a capacitor structure on a semiconductor substrate ... comprising ... forming at least one insulating sidewall spacer placed against said perimeter of said top plate and overlying a portion of said dielectric layer” (emphasis supplied).

With respect to this feature, paragraph 9 of the present Office Action cites *Lee*’s sidewall spaces 70 shown in Figures 4-6. However, it is evident from the above-noted figures of *Lee* that sidewall spacers 70 do not overlay a portion of dielectric layer 30. The Examiner seeks to dismiss this omission of *Lee* by attempting to equate the word against with the word overlying (viz. “forming insulating sidewall spacers 70 ... **against or overlying** a portion, i.e. outer perimeter, of the dielectric layer 30”, Office Action, page 4, lines 5-7). This attempted linguistic legerdemain does not change the fact that in the semiconductor industry overlay and thus overlying always refers to vertical stacking of layers along the Z axis orthogonal to the semiconductor substrate, as evidenced by the attached sampling of definition and articles. There is no evidence that abutting features along the X or Y axes are considered to be overlying as that term is employed in the semiconductor arts and the present specification.

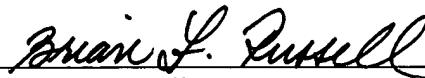
Because *Lee* and the other references of record fail to disclose “forming at least one insulating sidewall spacer placed against said perimeter of said top plate and overlying a portion of said dielectric layer” as recited in exemplary Claim 9, Applicant believes that the rejections of Claim 9 and its dependent claims set forth in the present Office Action are overcome and all pending claims are in condition for allowance.

Applicant further believes that the rejections of Claims 18-19 are overcome because *Lee* and the other references of record do not disclose “forming at least one insulating sidewall spacer on a top surface of the dielectric layer.” At page 4 of the present Office Action, *Lee*’s second dielectric layer 80 is cited as teaching the claimed at least one insulating sidewall spacer. However, layer 80, although overlying *Lee*’s dielectric layer 30, is not formed “on a top surface” of dielectric layer 30 as required by the present claims, as can be clearly see from *Lee*’s Figure 5. Consequently, the Examiner’s rejections of Claims 18-19 are not well founded and should be withdrawn.

Having now responded to each objection and rejection set forth in the present Office Action, Applicant believes all pending claims are now in condition for allowance and respectfully requests such allowance.

No additional fee is believed to be required; however, in the event any additional fees are required, please charge IBM Corporation Deposit Account No. **09-0456**.

Respectfully submitted,

A handwritten signature in cursive script, reading "Brian F. Russell", is written over a horizontal line.

Brian F. Russell
Registration No. 40,796
BRACEWELL & PATTERSON, LLP
P.O. Box 969
Austin, Texas 78767
(512) 472-7800

ATTORNEY FOR APPLICANT